Actions-micro AM8372 Datasheet

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Document Number: AM8372 Datasheet
Revision 1.0.0
Release date: 2023.06

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Revision History

Version	Date	Description	Author
1.0.0	2023.06	Initial Create	maweishuo

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Terms and Acronyms

Terms and Acronyms	

Block Diagram

AM8372 BLOCK DIAGRAM

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2 Feature

The AM8372 provides high level of system integration to support a wide variety of applications. The features of the AM8372 include:

32BIT RISC CORE

- 32K byte instruction cache and data cache
- F/W can program from DC up to 800MHz transparently
- DSP instruction for multi-media acceleration
- Static design allows changing clock at run-time for power saving

VIDEO ENCODER

- 60 frames per second at 1920x1080 resolution for video all format

IMAGE/VIDEO COMPRESSOR

- Support upto 1080P Resolution
- Support 8bit YCbYCr/RGB
- Adaptive compress ratio up to 1:6
- Lossless or Near-lossless compress

OSD

- 1,2 OSD bitmap data width
- 256x128 size in 2 bit or 256x256 in 1 bit

DISPLAY INTERFACE

- HDMI Tx support, iP0.825 0 Td(MI)Tj1.2Td4Td(-)Tj/TT3 14.2Td4 Tf1.375 0 Td 1I

DMA CONTROLLER

- 8 physical channels and 4 bus channels
- Stride mode support
- Software configurable priority

Boot ROM

- On chip boot ROM with boot loader
- The system could be loaded from SPI Nor flash

USB 2.0 OTG

- Complies with Universal Serial Bus Specification. Revision 2.0.
- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a.
- Supports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode.
- Supports full-speed or high-speed in peripheral mode.
- Supports USB Mass Storage Class Bulk-Only Transport Revision 1.0 as host or device.
- Supports Electronic still picture imaging Picture Transfer Protocol (PTP)
- Supports direct print function using pict-bridge
- Supports Universal Serial Bus Device Class Definition for Printing Devices Version 1.1 as host
- Supports Universal Serial Bus Still Image Capture Device Definition Revision 1.0 as host
- Configurable/proge[illegible]

3 Power on Sequence

The power on sequence requirements of the AM7xxx and AM8xxx products are the same, which are shown in the following figure. VDD represents the power pins supplying power for the core. VCC represents the power pins supplying power for the general purpose pads. SVCC represents the power pins supplying power for the DDR2 or DDR3 SDRAM related pads. P_RESETB is the asynchronous reset pin. PWROK is an internal signal. It is low during the power-on phase to reset all the registers in the chip. The system boots at the moment when PWROK turns to high.

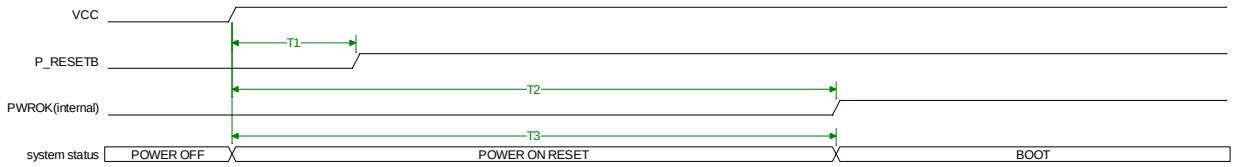

Figure 1 Power on Sequence Diagram

Timing Requirements:

1. 1 20

4 Pin Out Specification

Pin out table

PIN NUM	PIN NAME	TYPE	Function
1	P_SPINSS	B	SPI_NSS
2	VCC3	PWR	VCC3
3	DVCC_PLL	PWR	AVCC_PLL2
4	HOSCI	A	HOSCI
5	HOSCO	A	HOSCO
6	AVCC2	PWR	AVCC2
7	VDD	PWR	VDD
8	EXT_R	A	EXT_R
9	AVDD33	PWR	AVDD33
10	RXCN_CH	A	RXCN_CH
11	RXCP_CH	A	RXCP_CH
12	RX0N_CH	A	RX0N_CH
13	RX0P_CH	A	RX0P_CH
14	RX1N_CH	A	RX1N_CH
15	RX1P_CH	A	RX1P_CH
16	RX2N_CH	A	RX2N_CH
17	RX2P_CH	A	RX2P_CH
18	AVDD12	PWR	AVDD12
19	HDMI_ON0	A	HDMI_ON0
20	HDMI_OP0	A	HDMI_OP0
21	AVCCPLL	PWR	AVCCPLL
22	HDMI_ON1	A	HDMI_ON1
23	HDMI_OP1	A	HDMI_OP1
24	HDMI_ON2	A	HDMI_ON2
25	HDMI_OP2	A	HDMI_OP2
26	DVCCPAD	PWR	DVCCPAD
27	HDMI_ON3	A	HDMI_ON3
28	HDMI_OP3	A	HDMI_OP3
29	CECTX	A	CEC_DAC
30	CECRX	A	CEC_DAC
31	P_I2C1SCL	B	I2C1SCL
32	P_I2C1SDA	B	I2C1SDA
33	VCC1	PWR	VCC1
34	P_RESETB	B	RESETB
35	P_UARTTX1	B	GPIO17

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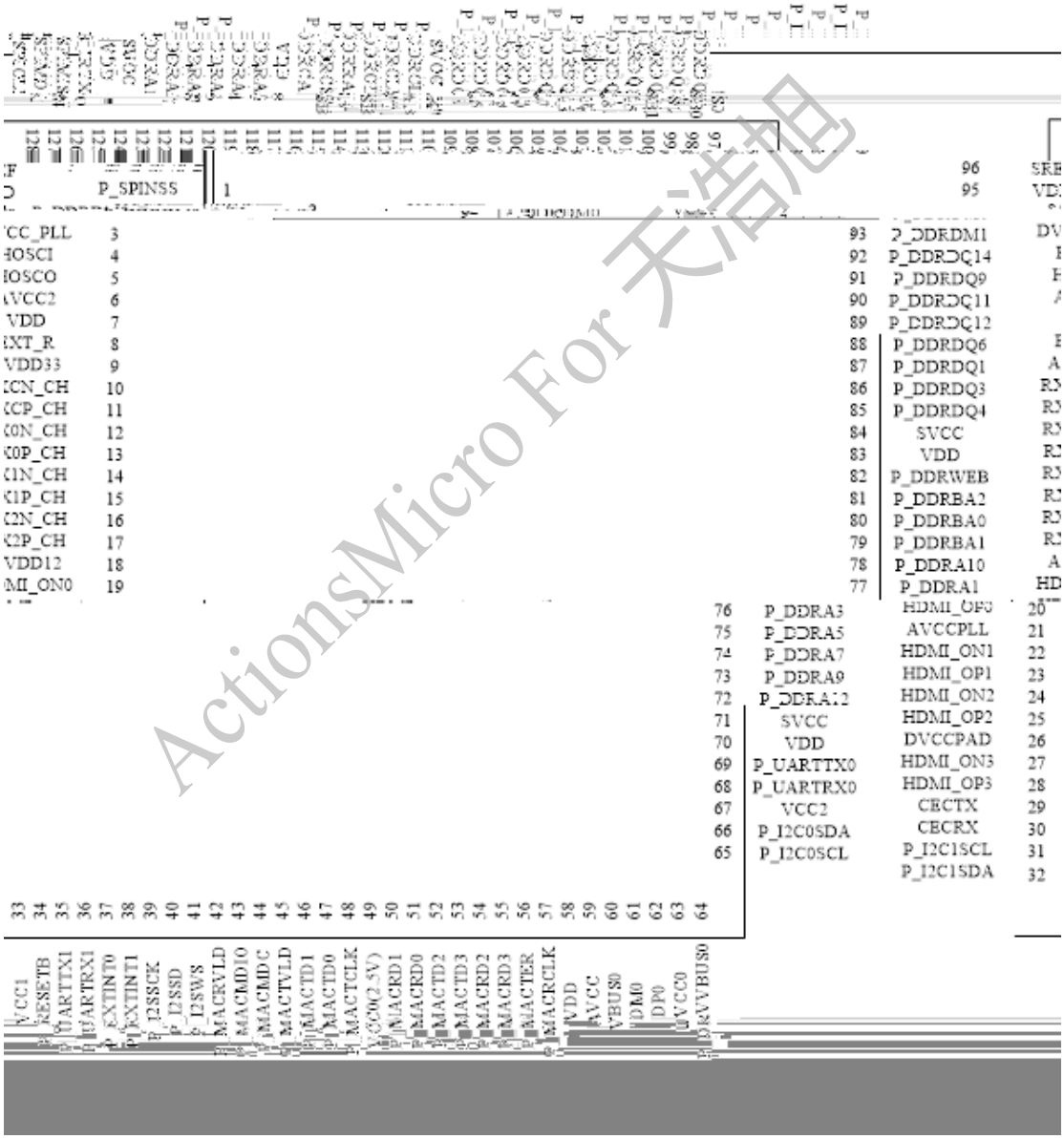
36	P_UARTRX1	B	GPIO18
37	P_EXTINT0	B	EXTINT0
38	P_EXTINT1	B	GPIO32/I2STMCLK
39	P_I2SSCK	B	I2SSCK/IRRX
40	P_I2SSD	B	I2SSD/I2STSD
41	P_I2SWS	B	I2SWS/I2STWS
42	P_MACRVLD	B	RGMII_RXCTL
43	P_MACMDIO	B	MACMDIO
44	P_MACMDC	B	MACMDC

79	P_DDRBA1	B	P_DDRBA1
80	P_DDRBA0	B	P_DDRBA0
81	P_DDRBA2	B	P_DDRBA2
82	P_DDRWEB	B	P_DDRWEB

122	P_DDRA11	B	P_DDRA11
123	SVCC	PWR	SVCC
124	VDD	PWR	VDD
125	P_IRTX	B	IRTX/I2STSCK
126	P_SPIMISO	B	SPI_MISO
127	P_SPIMOSI	B	SPI_MOSI
128	P_SPICLK	B	SPI_CLK



AM8372 PIN-OUT DIAGRAM

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5 Operating Conditions

Absolute Maximum Ratings

SYMBOL			
V_{CC}	Power Supply (3.3V)	3.8	V
Vsvcc	Power Supply (1.5V)	1.575	V
V_{dd}	Power Supply (1.35V)	1.4	V
V_{IN}	Input Voltage	-0.5~4.6	V
V_{OUT}	Output Voltage	-0.5~4.6	V
T_{STG}	Storage Temperature	0~75	
Tc	Operation Temperature (Case Surface)	0~70	
Ta	Ambient Temperature	0~60	

Recommended Operation Conditions

V_{CC}	Power Supply (3.3V)	3.0	3.3	3.6	V
Vsvcc	Power Supply (1.5V)	1.425	1.5	1.575	V
V_{dd}	Power Supply (1.35V)	1.3	1.35	1.4	V
T_a	Ambient Temperature	0	35	60	

DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V_{CC} = 3.0V~3.6V, T_j = 0 to +70)

V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.2			V
V_{T-}	Schmitt Input Low Voltage				0.9	V
V_{T+}	Schmitt Input High Voltage		1.9			V
V_{OL}	Output Low Voltage	4mA			0.4	V
V_{OH}	Output High Voltage	4mA	2.4			V 4m

6 Crystal Requirements

Requirements for 24MHz oscillator.

Description	Specification Requirement
Nominal Frequency	24MHz
Oscillation Mode	Fundamental
Frequency Tolerance at 25	± 30ppm
Temperature Stability	± 50ppm
Shunt Capacitance (Co)	7pF max
Load Capacitance (CL)	12pF~18pF
Equivalent Series Resistance (ESR)	50ohm max
Drive Level	500uW max
Aging (at 25)	± 3ppm/year
Insulation Resistance	10meg
Net Weight	This will be various. No limitation.
Operating Temperature Range	-10~85
Storage Temperature Range	-45~125

Requirements for 32.768KHz oscillator.

Description	Specification Requirement
Nominal Frequency	32.768KHz
Oscillation Mode	Fundamental
Frequency Tolerance at 25	± 30ppm
Temperature Stability	± 50ppm
Shunt Capacitance (Co)	7pF max
Load Capacitance (CL)	12pF~18pF
Equivalent Series Resistance (ESR)	50ohm max
Drive Level	500uW max
Aging (at 25)	± 3ppm/year
Insulation Resistance	10meg
Net Weight	This will be various. No limitation.
Operating Temperature Range	-10~85
Storage Temperature Range	-45~125

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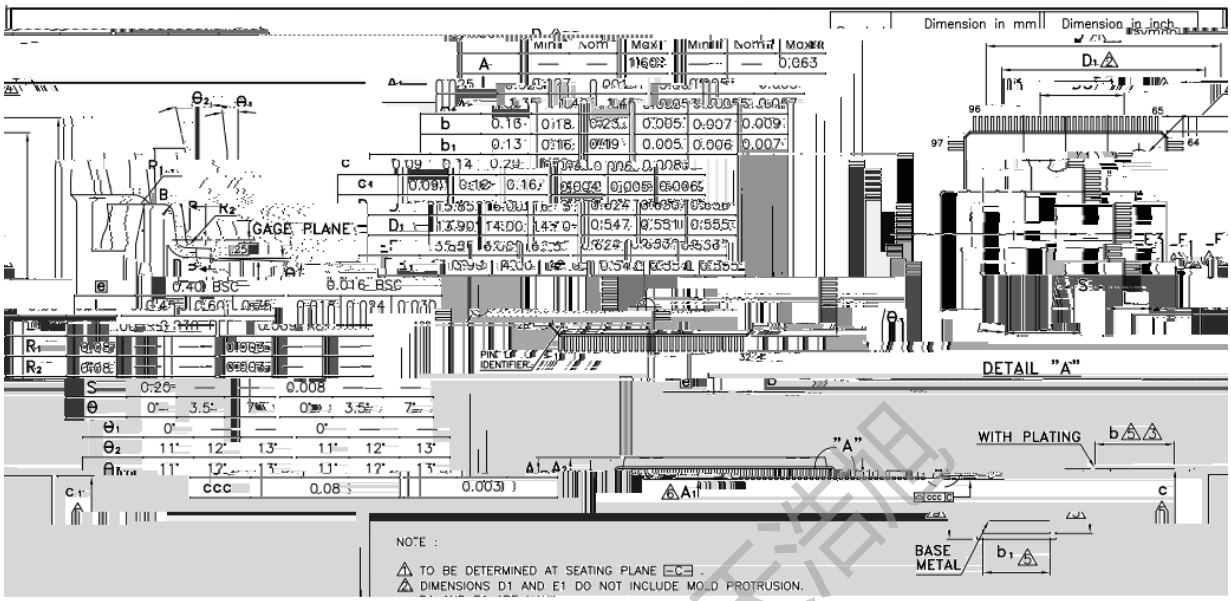
7 Mechanical Specification



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