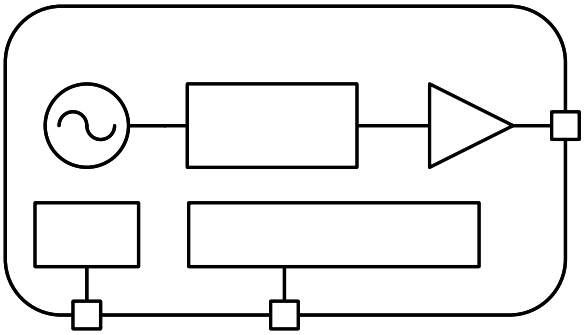
AS511 Low Jitter LVCMOS Silicon Oscillator

Description

The AS511 Arcadium™ all-silicon CMOS oscillator utilizes proprietary frequency synthesis and sensor technologies to provide a quartz-free, MEMS-free, low jitter clock at any output frequency. The device is factory-programmed to a fixed frequency ranging from 10 kHz to 212.5 MHz with 0.026 ppb resolution and maintains low jitter across its operating range.It uses on-chip temperature and strain sensors, and an advanced LC tank architecture to achieve excellent reliabilities even in high impact shock scenarios.

AS511's on-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in an industry-standard 3225 and 5032 package, the AS511 has a dramatically simplified supply chain that enables Aeonsemi to ship samples shortly after receipt of order. Specific frequency and OE/ACT are factory programmed at time of shipment, eliminating the long lead times associated with custom frequencies. This process also guarantees 100% electrical testing of every device before shipment.



Key Features

Quartz-free and MEMS-free without mechanical moving parts

LVCMOS output: 10 kHz to 212.5 MHz

Low jitter: 350 fs Typ
(12 kHz – 20 MHz, @156.25 MHz)

Temperature stability:

– ±20 ppm (-20 to 85 °C)
– ±35 ppm (-40 to 85 °C)
– ±35 ppm (-40 to 105 °C)

Integrated LDO for on-chip power supply noise filtering

Support 1.8V, 2.5V, 3.3V V_{DD} supply operation

Industrial standard 3225 and 5032 package footprints

Application

1G/10G/40G/100G/200G Ethernet

Servers, switches, storage, NICs, search accel-

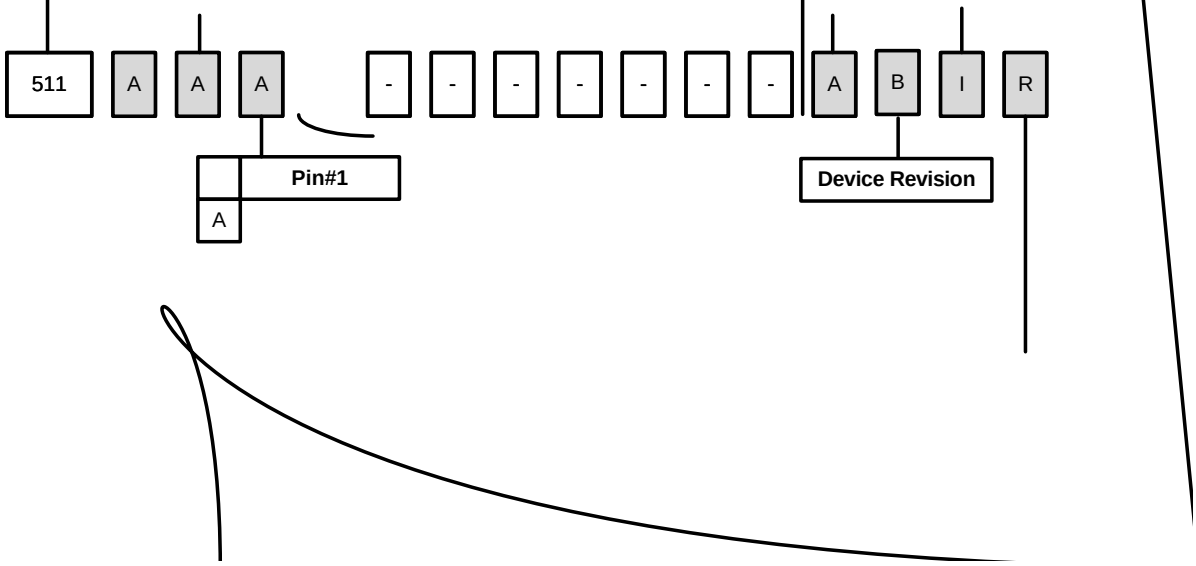
1. Ordering Guide

XO Series	Description
511	CMOS Oscillator

	Device Type
A	General

	Package
A	5032

	Temperature Grade
I	-40 to 85 °C



Note:

1. “X” refers to the ID for the unique configuration with factory-defined settings, the value ranges from “B” to “Z”.
2. For example: 125 MHz = 125M0000; 33.33333 MHz = 33M33333.

2. Electrical Specifications

Table 2.1. Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Note
Operating Temperature Range						
Temperature Range	T_A	-40	—	85	°C	Industial grade
		-40	—	105	°C	Extended industial grade
Supply Voltage and Power Consumption						
Supply Voltage	V_{DD}	1.71	—	3.47	V	
Supply Current (F_{CLK} = 50 MHz)	I_{DD}	—	40	50	mA	Tristate Hi-Z (OE = 0)
		—	1	2	mA	Ready State (ACT = 0)
		—	40	55	mA	LVCMOS output (C_L = 15 pF)
Frequency Range						
Frequency Range	F_{CLK}	0.01	—	212.5	MHz	LVCMOS output
Frequency Tolerance						
Initial frequency accuracy	F_{INIT}	-10	—	10	ppm	Inclusive of initial frequency tolerance at 25°C and variations over supply voltage, load and humidity after soldering-reflow shift settles.
Temperature stability	F_{STAB}	-20	—	20	ppm	-20 - 85°C
		-35	—	35	ppm	-40 - 85°C
		-35	—	35		

Parameter	Symbol	Min	Typ	Max	Unit	Note
Phase Noise and Jitter						

3. Package Outline Drawing

Figure 3.1. shows the package outline drawing for the AS511 devices. Details of dimension for different size options are listed in Table 3.1.

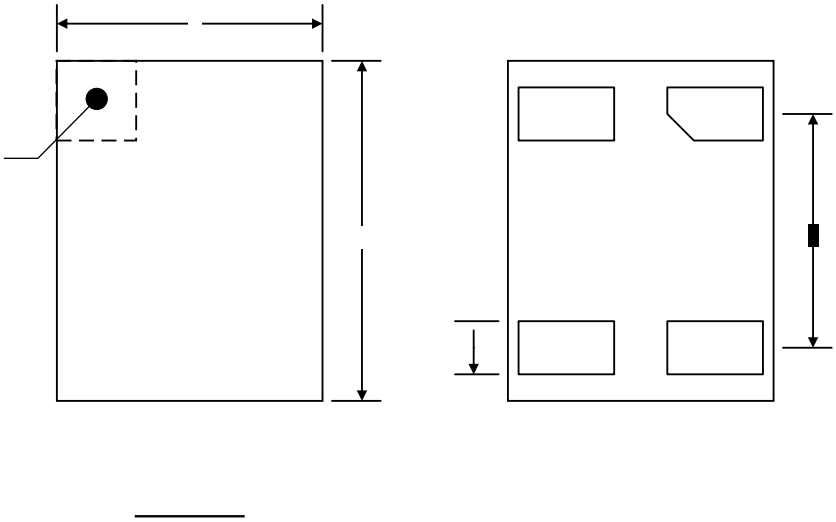


Figure 3.1. Package Outline Drawing

Table 3.1. Dimensions of Package Outline Drawing (mm)

Symbol	5032 Package	3225 Package
A	0.85 ± 0.05	0.85 ± 0.05
b	0.64 ± 0.05	0.90 ± 0.05
D	3.20 ± 0.10	2.50 ± 0.10
e	2.54 BSC	2.10 BSC
E	4.00 ± 0.10	3.20 ± 0.10
L	0.94 ± 0.05	0.70 ± 0.05
L1	0.10 ± 0.05	0.10 ± 0.05

4. Recommended PCB Land Pattern

Figure 4.1. shows the drawing of recommended PCB land pattern for the AS511 devices. Details of dimension for different size options are listed in Table 4.1.

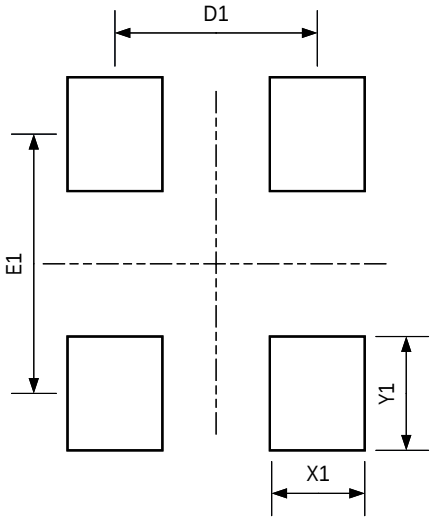


Figure 4.1. Recommended PCB Land Pattern

Table 4.1. Dimensions of Recommended PCB Land Pattern (mm)

Symbol	5032 Package	3225 Package
D1	2.16	1.70
E1	2.54	2.10
X1	1.24	1.00
Y1	0.84	1.10

Notes:

The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Materim70msondilication MMC50mm.Thisum Materim70msondilic8(tation)-278(LMC50mmsign)-278

5. Top Mark

Figure 5.1.

6. Packing Specification

Figure 6.1. shows the packing specifications for the AS511 devices. Details of the tape specifications are listed in Table 6.1.

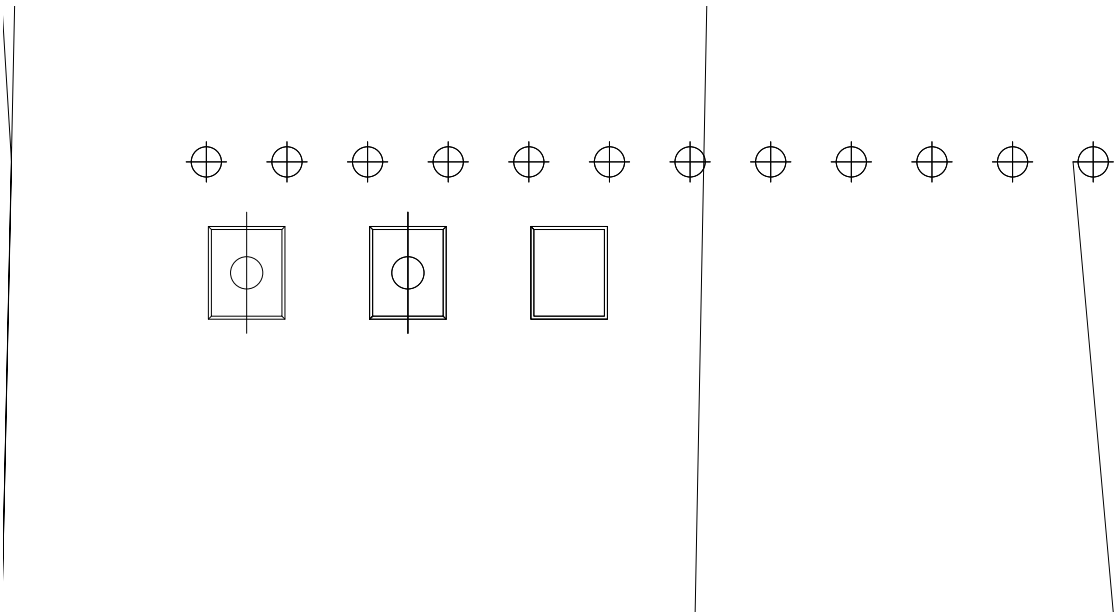


Figure 6.1. Tape Specification

Table 6.1. Dimensions of Tape (mm)

Symbol	5032 Package	3225 Package
A0	3.50 ± 0.10	2.80 ± 0.10
B0	4.30 ± 0.10	3.50 ± 0.10
K0	1.25 ± 0.10	1.05 ± 0.10
E1	1.75 ± 0.10	1.75 ± 0.10
F	5.50 ± 0.05	5.50 ± 0.05
W	12.00 ± 0.30	12.00 ± 0.30
T	0.30 ± 0.05	0.30 ± 0.05
P0	4.00 ± 0.10	4.00 ± 0.10
P1	8.00 ± 0.10	8.00 ± 0.10
P2	2.00 ± 0.05	2.00 ± 0.05
ØD0	1.50 ± 0.10	1.50 ± 0.10
ØD1	1.60 ± 0.10	1.60 ± 0.10

7. Important Notice and Disclaimer

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8. Revision History

Revision	Date	Description
1.13	Aug 2025	Corrected the tape specification
1.12	Aug 2024	Add packing specification
1.11	Mar 2024	Updated the frequency offset
1.10	Jul 2022	Updated the top mark specification
1.01	Dec 2021	Adjusted the PCB land pattern dimensions
1.00	Sep 2021	With certain specification update
0.95	Jun 2021	Corrected the Ordering Guide Insert -40 - 105 °C temperature range option Insert section “IMPORTANT NOTICE AND DISCLAIMER”
0.20	Mar 2021	Changed the frequency range and ordering guide
0.10	Feb 2021	Initial release