12-Channel 1:2 MUX/DEMUX

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TRADEMARKS

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REVISION HISTORY

Revision	data	Summary
V1.0	2023.02.22	Draft released Dra2[illegible]

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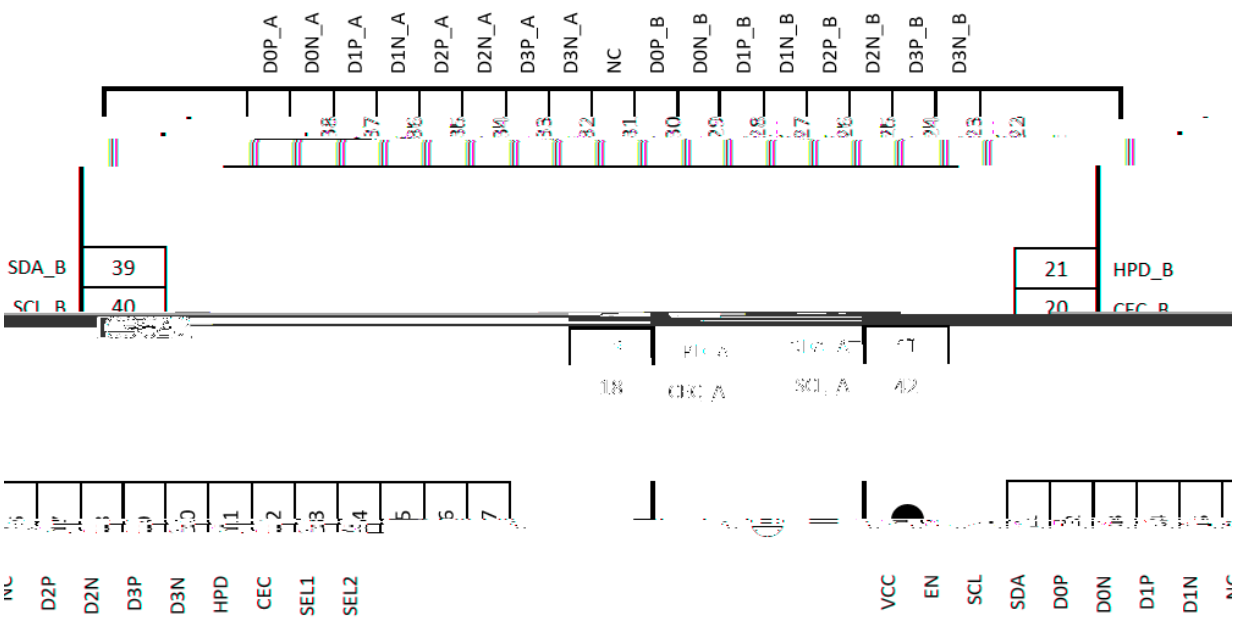
3.1 Pin Assignment



4. System Functional Descriptions

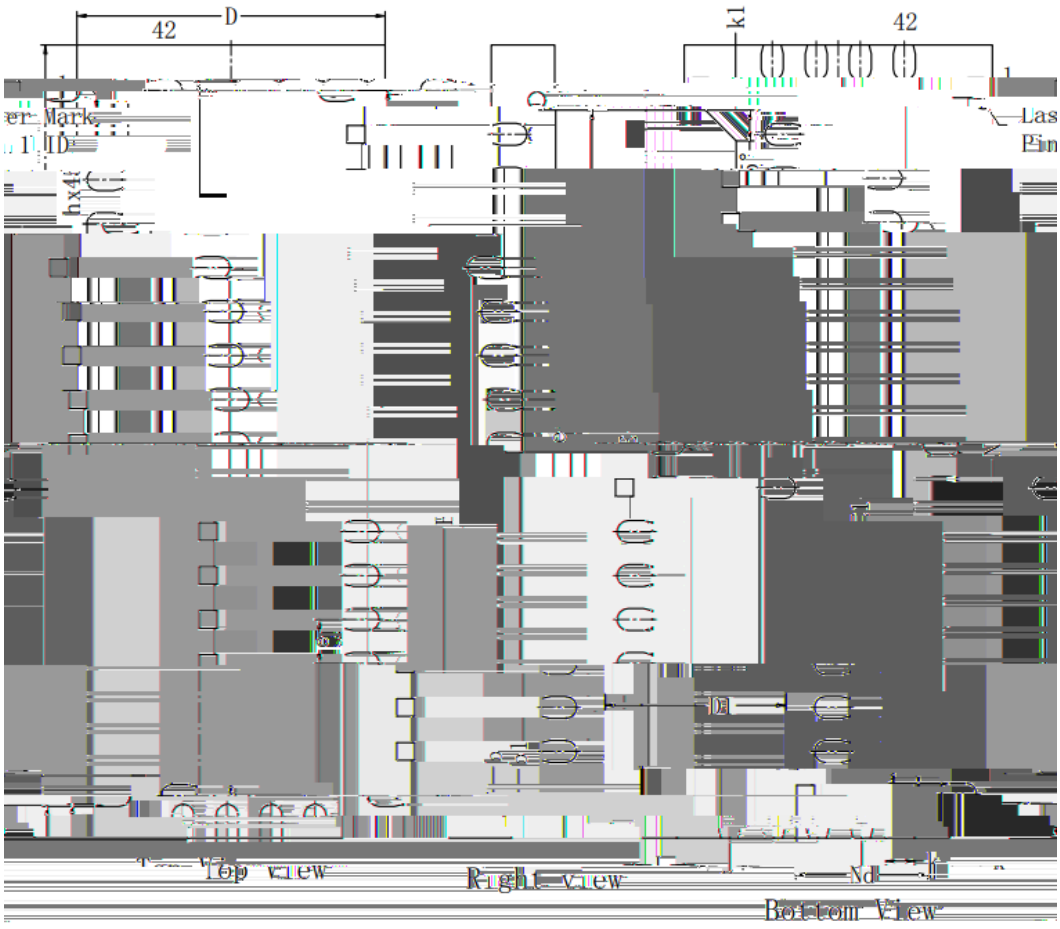
4.1 Functional Block Diagram

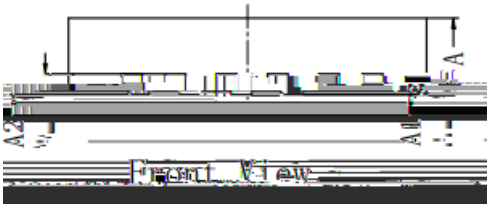
4.2 Device Functional Modes

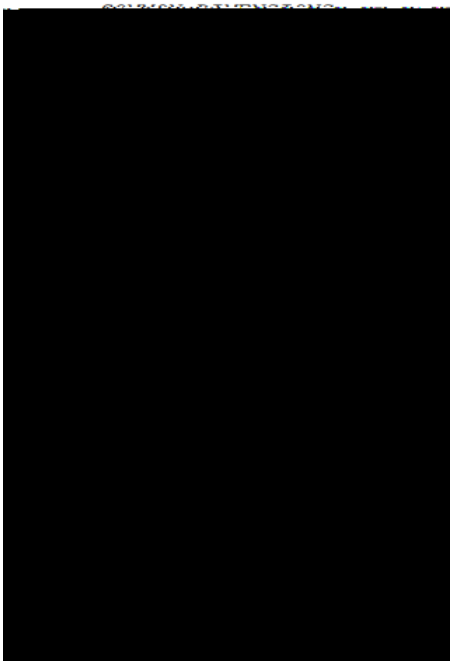
5.3 Switching Characteristics

PARAMETER				TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}			All I/O				110	µs
t_{SWITCH}			All I/O			30		µs
t_{pd} Propagation Delay		Port A	D0 to D3			40		ps
			SCL, SDA, HPD, CEC			40		
		Port B	D0 to D3			50		
			SCL, SDA, HPD, CEC			40		
t_{SKEW}	Inter-pair Skew	Port A	D0 to D3	Between positive and negative signals of each Channel		3		ps
		Port B				3		
	Intra-pair Skew	Port A						

6. Mechanical Information







7.3 Layout Application